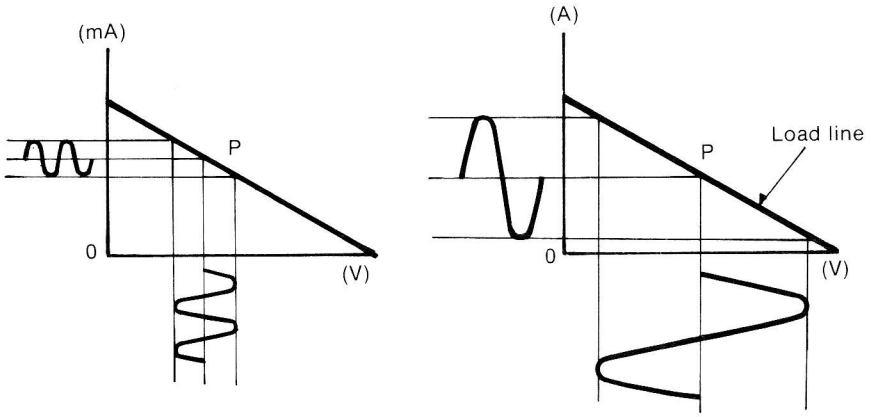
15. POWER AMPLIFIER CIRCUIT

Sound signals amplified by the audio frequency amplifier circuit are amplified again by the power amplifier so they have enough power to drive the speaker.
A small signal amplifier circuit treats low-level signals and utilizes only a small part of the transistor's potential, while a power amplifier circuit utilizes virtually all of a transistor's potential to obtain a large output.



(a) Small signal amplification. (b) Large signal amplification

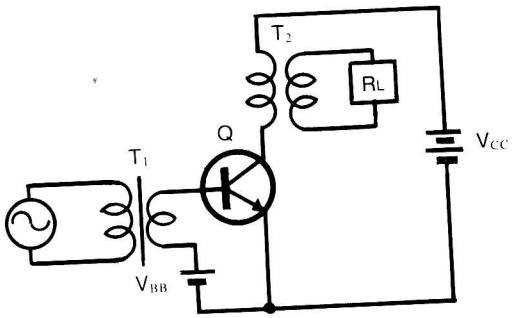
[Fig. 15-1]

To use most of a power amplifying transistor's potential, relatively large input signals are required. Even when a detector output is applied directly to a power amplifier circuit, a sufficient output cannot be obtained and the transistor is insufficiently used. Therefore, the detector output must be first amplified by a small signal amplifier and then be applied to the power circuit.
Additionally, the power circuit controls the collector current to obtain a large output. For that purpose, its circuit configuration differs from a small signal amplifier circuit in the following ways.
If there is a resistance on the output side, such as in a RC connection circuit, power loss due to the resistance increases.
To minimize the loss, the power circuit is provided with a transformer connection circuit, push-pull circuit, etc.
Power circuits are classified into two types: Class A power amplification circuits and Class B push-pull circuits.

- Class A power amplifier circuit:
  Transistor working point is approx. at the center of the load line.
- Class B push-pull circuit:
  Transistor working point is at the cut-off point. Two transistors are combined.

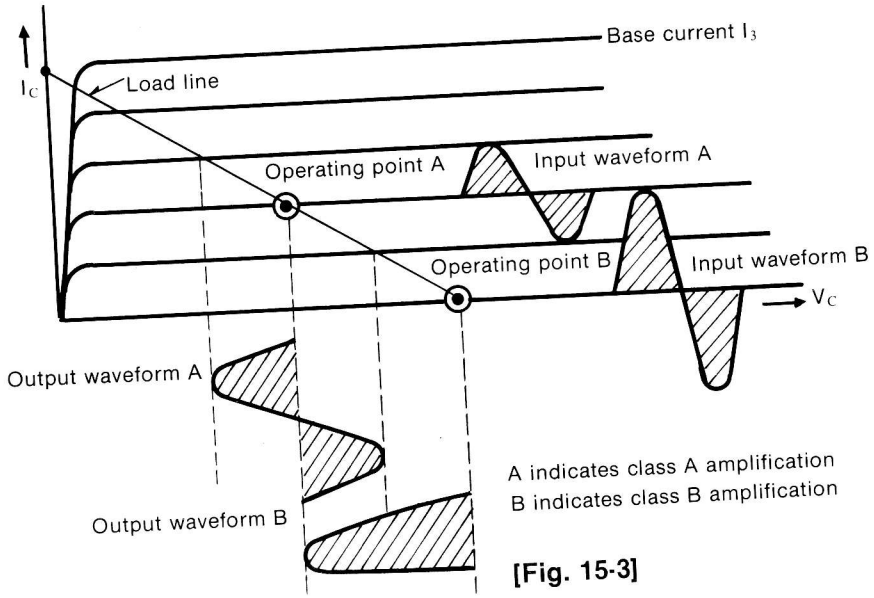
15-1. Class A Amplifier Circuit

(1) Theoretical circuit

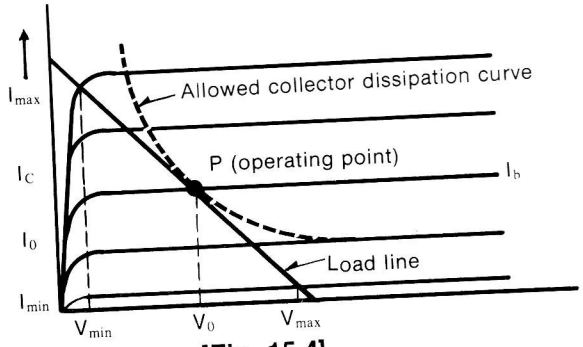


[Fig. 15-2]

[Fig. 15-2] shows a basic Class A power amplifier circuit which composes a transformer connection circuit. Transformer T_2 is referred to as "output transformer" which provides the optimum load to the transistor for obtaining a desired output as well as supplying transistor output to load resistor R_L effectively. Transformer T_1 is referred to as "input transformer", which performs matching between signal source internal resistance (output impedance of the former stage) and transistor impedance for more effective signal transmission. Power efficiency of Class A power amplifier circuits has a theoretical maximum of 50%. The DC power source supplies power, 50% of which is taken out by load R_L as output power, and 50% of which is consumed by transistor collector dissipation as heat. In actual cases, power efficiency is lower than the above figures. A power efficiency of 50% can be obtained only in theoretical transistor and transformer applications.



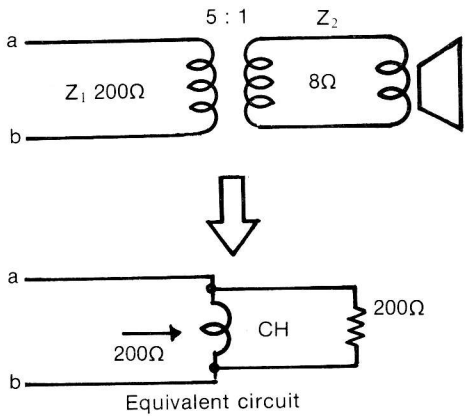
[Fig. 15-3]



[Fig. 15-4]

- An amplifier circuit, in which the operating point is chosen at the middle of the load line as shown in [Fig. 15-3], is called a class A amplifier circuit.
- Maximum output can be obtained when a load value is determined so that the load line contacts the allowed collector dissipation curve.

(2) Single type



[Fig. 15-5]

The ideal output transformer, used for impedance matching of the output circuit, is 0Ω at DC and ∞Ω at AC. Also, the current and voltage can be effectively used without any drop.

As a matching transformer, the necessary impedance of the primary with an 8Ω secondary can be obtained by the winding ratio. The relation is calculated as

$$Z1 = \frac{N_1}{N_2}^2 \cdot Z_2$$

and it can be chosen to be any arbitrary value.

N_1 = Number of primory turns

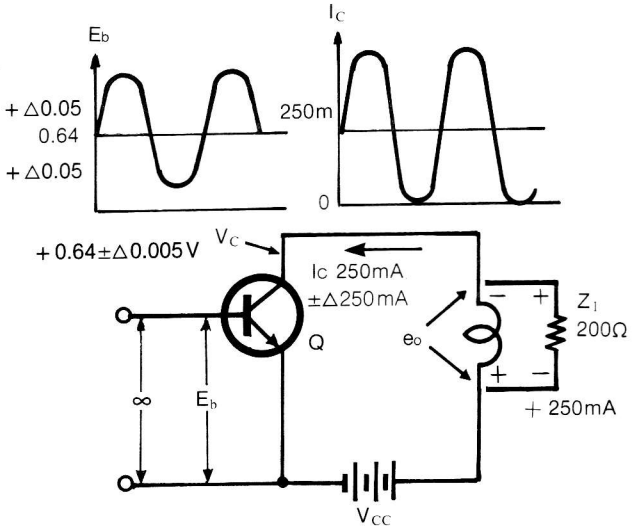
N_2 = Number of secandary turns

Z_1 = Primory impedance

Z_2 = Secandary impedance

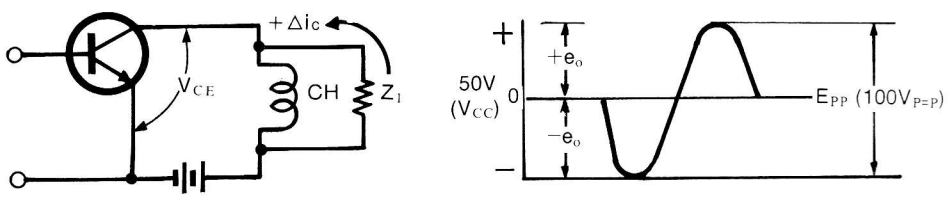
For example in a class A amplifier circuit, if there is a ±0.05V voltage variation (input signal) at the base-emitter, the collector current varies ±250mA from the standard 250mA. For example when it is +△250mA, a reverse voltage appears at Z1. Since its polarity is the same with V_{CC}, voltage V_C of Q is increased. Therefore, the maximum of V_C is

$$V_C = V_{CC} + e_o$$



[Fig. 15-6] Class A amplifier circuit

Therefore output voltage e_0 (peak to peak) can varies in level up to 2 times the maximum Vcc.

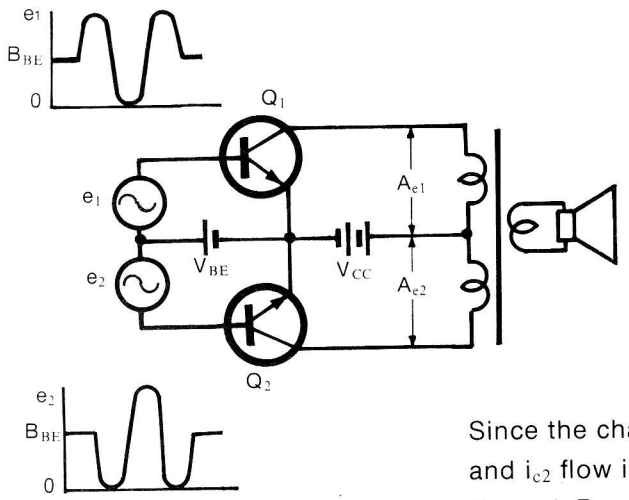


$$V_{CC} = e_o = \frac{E_{pp}}{2}$$

$$e_o + \Delta i_c Z_1$$

[Fig. 15-7]

(3) Class A push-pull amplifier circuit



(Fig. 21-8) Class A push-pull amplifier circuit

Although push-pull means that both transistors operate alternately, in a class A push-pull amplifier the phase of the inputs to Q1 and Q2 are made opposite and then amplified.

Since the characteristics of Q1 and Q2 are equal, $i_{c1} = i_{c2}$. i_{c1} and i_{c2} flow in the same direction with the same phase, flows through R_L and then drives the speaker. The relation between Z_1 and R_L is

$$2R_L = \ldots Z_1 \quad \therefore R_L = \frac{Z_1}{2}$$

Note: Z_1 = Load impedance for single type

R_L must be selected to be half the load impedance (Z_1) of the class A single type.

If this relation is ignored, distortion and output power are satisfied.

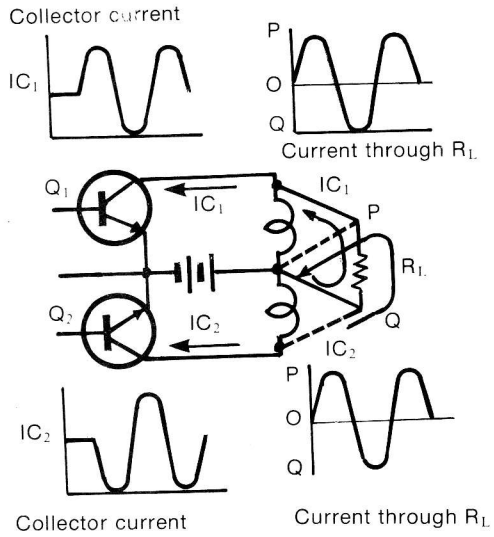
The push-pull output power (Pp) can be expressed as:

$$Pp = \frac{2V_{CC} \cdot 4I_C}{8}$$

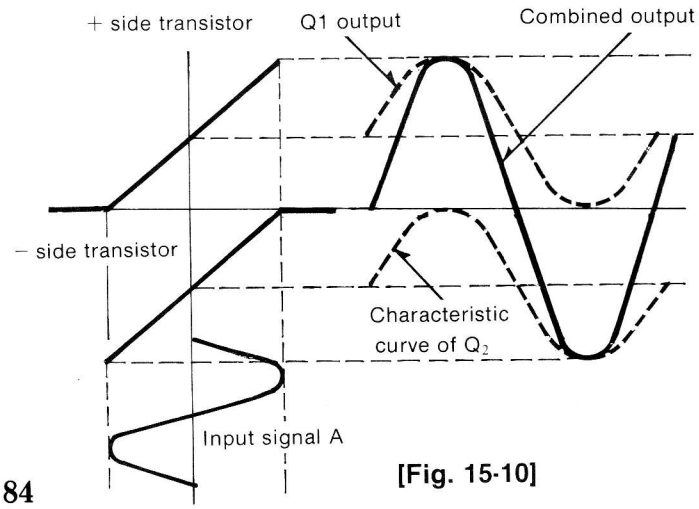
On the other hand, the output power of the single system (Ps) can be expressed as

$$Ps = \frac{2V_{CC} \cdot 2I_C}{8}$$

and when compared to push-pull, Pp/Ps = 2, the output of the class A push-pull amplifier is 2 times that of the single type.



[Fig. 15-9]



[Fig. 15-10]

Advantages

Since the transistor is always amplifying the signal as shown in Fig. 20-10, switching distortion is not generated.

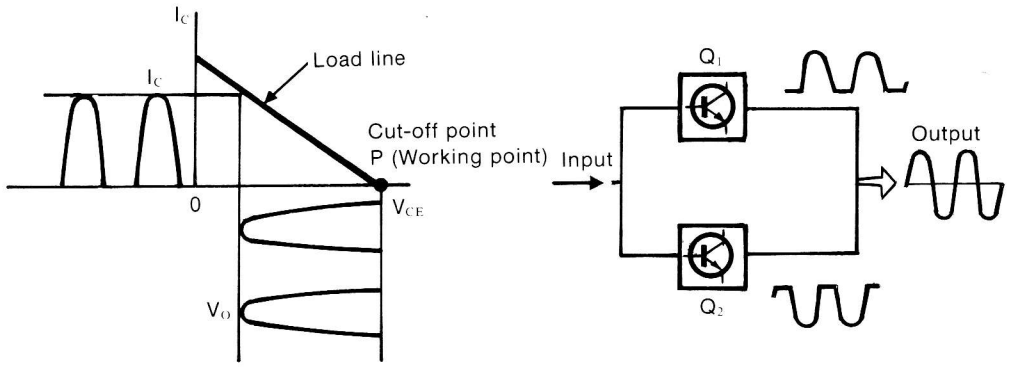
Disadvantages

Current must always flow through the transistor. As a result, much heat is generated and the power efficiency is greatly reduced.

15-2. Class B Amplifier Circuit

(1) Outline of Class B Amplifier Circuits

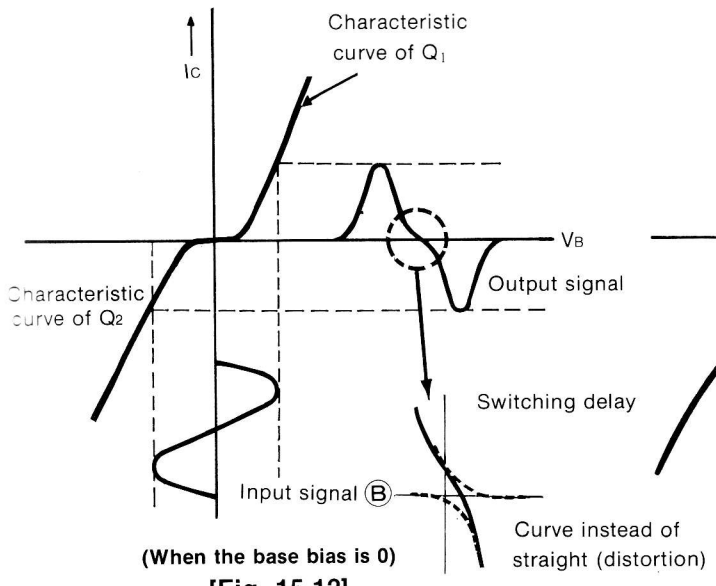
Push-pull amplifier circuits



[Fig. 15-11]

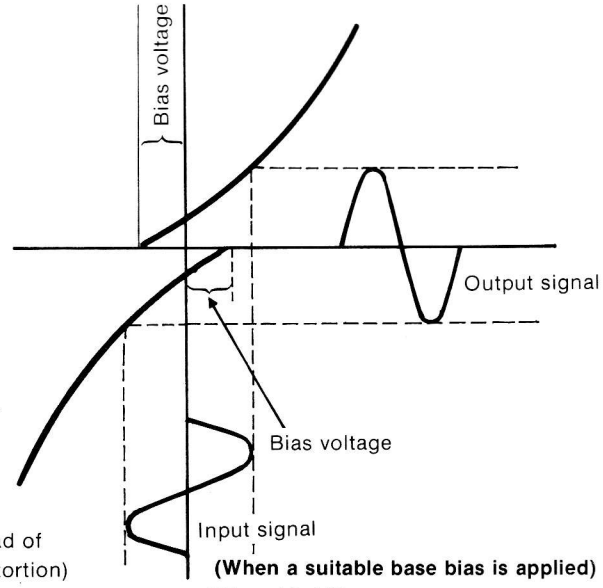
As shown in [Fig. 15-11 (a)], Class B power amplifier circuit, the transistor working point is set at the cut off point for amplification. Therefore, during one half-cycle of the input signal, the collector current flows and the output waveform becomes a half-wave. Therefore, identical input and output waveforms cannot be obtained.

To compensate for this, two transistors with the same characteristics are used. One amplifies the positive half of the signals and the other amplifies the negative half. As a result, the two amplified half-waves compose the output signal. In this way, very large outputs can be obtained.



(When the base bias is 0)

[Fig. 15-12]



(When a suitable base bias is applied)

[Fig. 15-13]

- Since the base bias current is 0, this circuit operates only during half the period of the input signals as shown in output waveform Ⓑ Since it cannot be used as it is, it is used in the push-pull amplifier circuit.
- Although as an advantage, its power efficiency is high, its disadvantage is that switching distortion is always generated due to its operation. This is because the 2 transistors operate alternately + to − and − to +.
  This switching does not occur smoothly and appears as distortion.
  This can be improved upon by applying a suitable a suitable base shown in [Fig. 15-13].

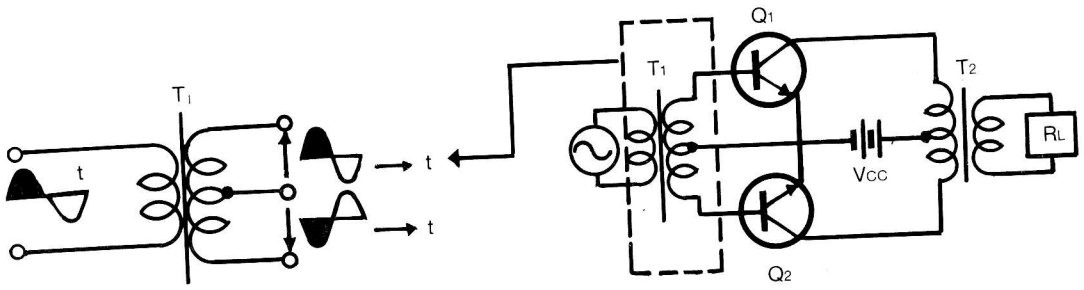
(2) Class B Push-Pull Amplifier Circuit

Typical Class B push-pull amplifier circuits are described below.

- **DEPP (Double Ended Push-Pull circuit**
  The most common type uses input and output transformers. In this type, the transformer is connected to two transistor's collectors.
- **SEPP (Single Ended Push-Pull) circuit**
  The speaker is connected to a point between the connecting point of two transistors and the earth. In this type, no output transformers are required. Therefore, it is referred to as "OTL (Output Transformer less)" type.

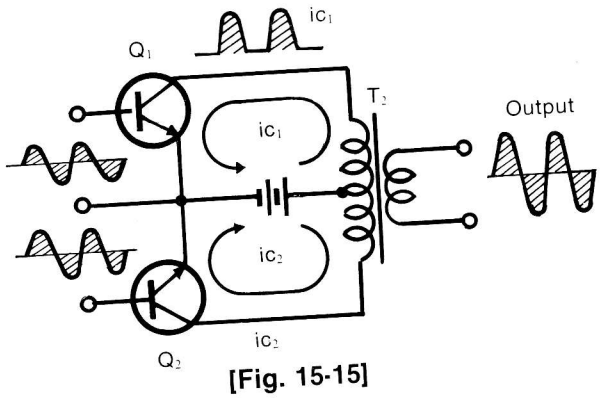
a) DEPP circuit

- **Operating principle of DEPP circuit**



[Fig. 15-14]

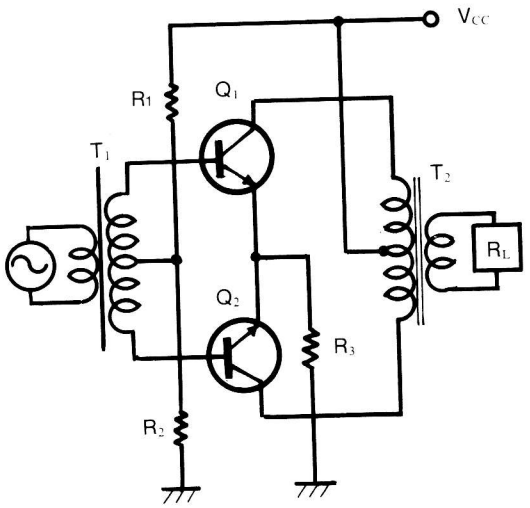
In a push-pull amplifier circuit, two opposite-phase signals are alternately applied to the two transistors to provide two alternate collector currents.



[Fig. 15-15]

When collector currents i_{C1} and i_{C2} flow through the center tap (common terminal) of transformer T_2, a composite output is obtained on the secondary side. This transformer is referred to as "output transformer". Input transformer T_1 provides two opposite-phase signals and matches the former stage with transistor input impedance. Output transformer T_2 is driven by two transistor outputs and provide a suitable impedance to Q_1 and Q_2. Therefore, transformers T_1 and T_2 must have a center tap. Power efficiency of Class B push-pull amplifier circuits are ideally at maximum of 78.5%. When there is no input signal, no collector current flows. Therefore, Class B power amplifier circuits are far more efficient than Class A circuit.

[Fig. 15-16] shows a typical Class B push-pull amplifying circuit.
To prevent crossover distortion, resistor R_1 and R_2 provide a slight bias to transistors Q_1 and Q_2.



[Fig. 15-16]

Since the two transistors operate alternately and their outputs are combined, if there are fluctuations in their characteristics such as h_{fe}, asymmetric distortion is produced in the output waveform.

Therefore, in push-pull amplifier circuits, two transistors with the same characteristics must be used.

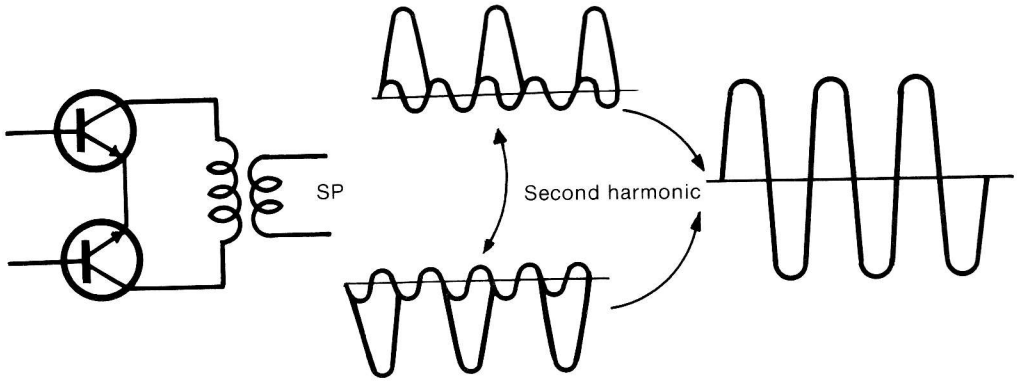
In a class B push-pull, V_{be} of Q1 and Q2 are selected to be near the cut-off point (actually a current is made to flow to eliminate the non-linear portion) and below this voltage, a current is not made to flow. In other words, class B only amplifies half a wave, so it cannot be used in a single type.

The output power Pp is

$$P_P \fallingdotseq \frac{2V_{CC}\ 4I_C}{8}$$

Therefore it is 2 times that of the class A single type.

Since the direction of current in the transformer is always opposite, DC magnetization is cancelled resulting in low distortion. The main advantage of the push-pull is that even harmonics are cancelled and distortion is eliminated as shown in [Fig. 15-17].

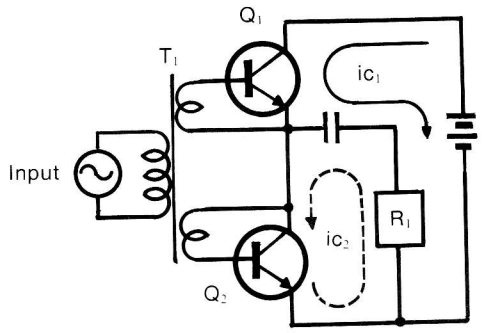


[Fig. 15-17]

b) SEPP circuit

Since DEPP circuits use input and output transformers, characteristics are degraded and circuit size and cost are increased.

To remedy this problem, a new push-pull circuit without transformers was developed.



[Fig. 15-18]

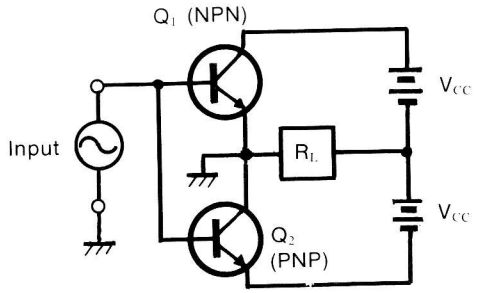
Dispensing with the output transformer, a transformer is used only in the input side and opposite-phase inputs are applied to transistors Q_1 and Q_2 for push-pull operation. Transistor output can be applied to load R_L through a capacitor without the need for an output transformer.

Such a circuit is referred to as "SEPP (Single Ended Push-Pull) circuit", or "OTL (Output Transformerless) circuit".

This circuit, however, requires a special transformer having two separated secondary windings, and therefore, it is not now used in practical applications.

(1)Complementary SEPP circuit

- **Outline of complementary SEPP circuit**



[Fig. 15-19] Complementary SEPP circuit

Use of PNP and NPN transistors having the same characteristic can allow push-pull operation without the need for input and output transformers.

A push-pull circuit combining PNP and NPN transistors having the same characteristic is referred to as "complementary SEPP circuit". This name is given because two transistors (PNP and NPN) have the same characteristics but the polarities, complementary.

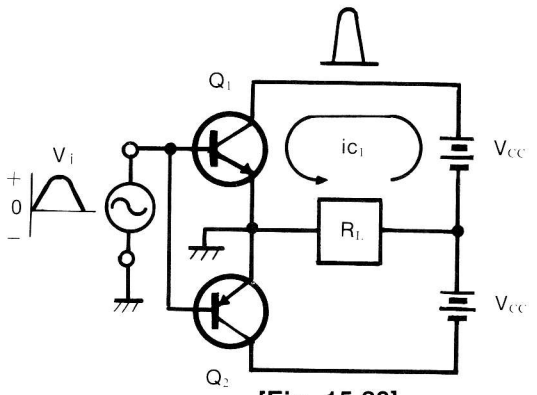
In this way, the two complementary transistors allow push-pull operation without the need for signal phase inversion by an input transformer.

Transistor output can be directly connected to load R_L without the need for a transformer.

- **Operating principle of complementary SEPP circuit**

  Q_1 in a complementary SEPP circuit is aPNP type. Q_1 and Q_2 bases are connected together and therefore receive the same input signal simultaneously.

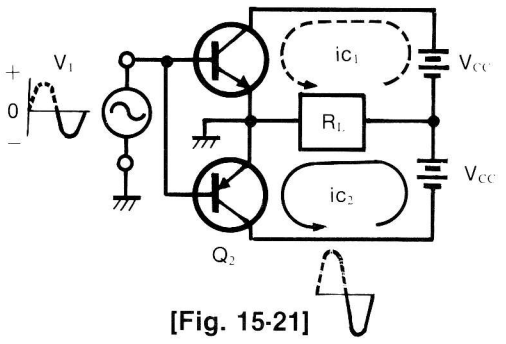
  Since, however, Q_1 is an NPN type, it operates when the base potential is positive with respect to the emitter. Q_2 is a PNP type and operates when the base potential is negative. That is, even if the same signal is applied to Q_1 and Q_2 simultaneously, only one of them operates at any one time. Therefore, as shown in [Fig. 15-20], when sine wave input V_i is applied, both base potentials become positive during the positive half cycle of V_i and only Q_1 (NPN) operates to allow collector current ic_1 to flow through load R_L. At that time, Q_2 (PNP) does not operate because of its reverse input.



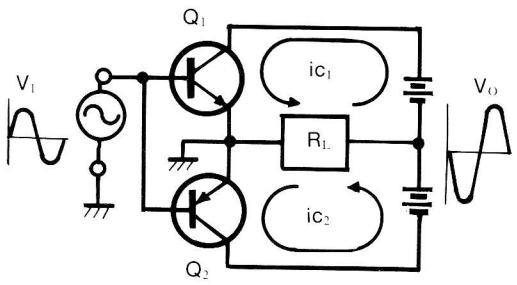
[Fig. 15-20]

During the negative cycle of input V_i, both bases are negatively biased. Therefore, only Q_2 (PNP) operates to allow collector current ic_2 to flow through R_L as shown in [Fig. 15-21]. Collector currents i_{C1} and i_{C2} flow in the opposite directions to provide an amplified sine wave output.

In other words, since Q_1 (NPN) and Q_2 (PNP) have opposite polarities, they alternately operate to complement each other and perform amplification.



[Fig. 15-21]



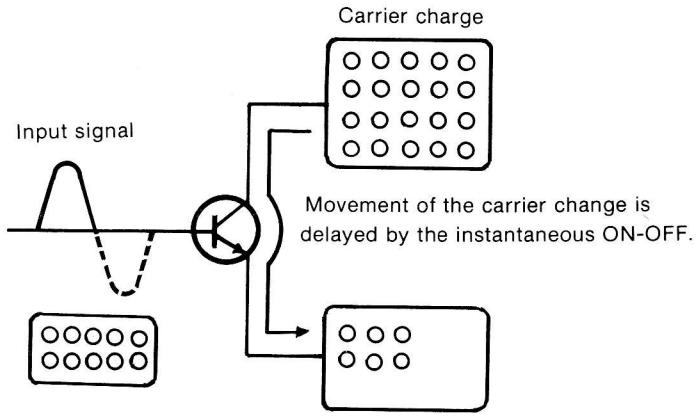
[Fig. 15-22]

- **Features of SEPP circuits**

  SEEP circuits have the following advantages compared with Class B push-pull amplifier circuit using input and output transformers, because their input and output transformers are larger, reduce low frequency gain and generate DC dissipation.

  1) Small circuit
  2) Economical
  3) Better frequency characteristics
  4) Improved power efficiency

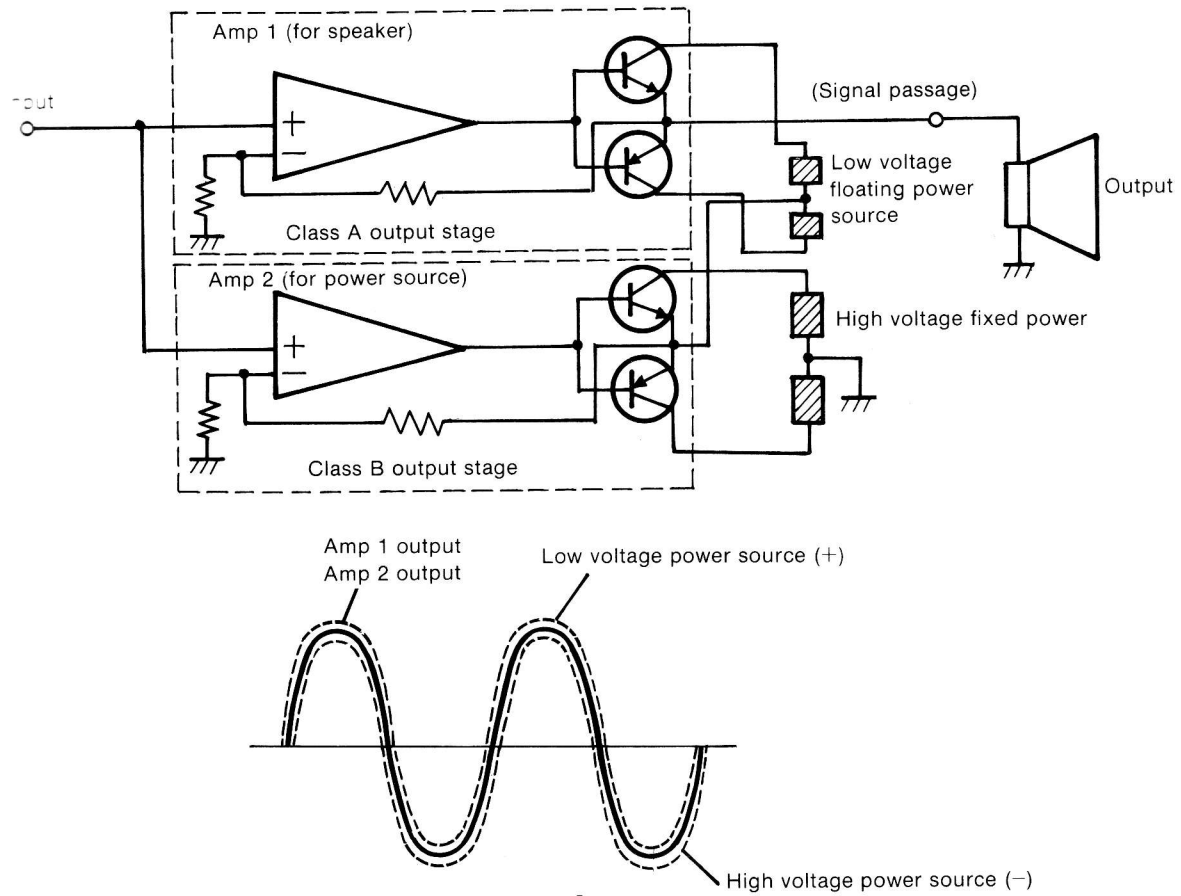
c) Desirable transistor for the class B amplifier



[Fig. 15-23] Movement of charge within the transistor

The higher the frequency of the signal, the harder it is for the transistor to keep up with the instantaneous ON-OFF switching. As a result, the movement of the carrier charge on the output side is delayed (distorted).
Although recently this has been improved by using transistors that can respond at high speeds to high frequencies, the delay cannot be completely eliminated in class B amplifiers.

15-3. Class A+



[Fig. 15-24]

- **Class A+ amplification**

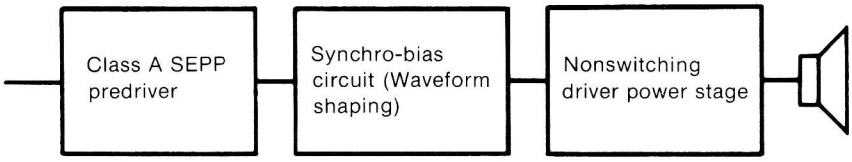
  It is the minimum requirement for class A operation to allow idling current of at least 1/2 of the peak current at the maximum output and to use only thelinear range of the output amplifying element. Therefore, to readuce the heat generation while satisfying these requirements, the supply voltage must be lowered.

  However, simply lowering the supply voltage is not sufficient since the output transistor is saturated on to allow power generation. To prevent this saturation, the collectoremitter voltage of the transistor is kept constant by making the power source floating at the central point and by driving the central point with the second amp.

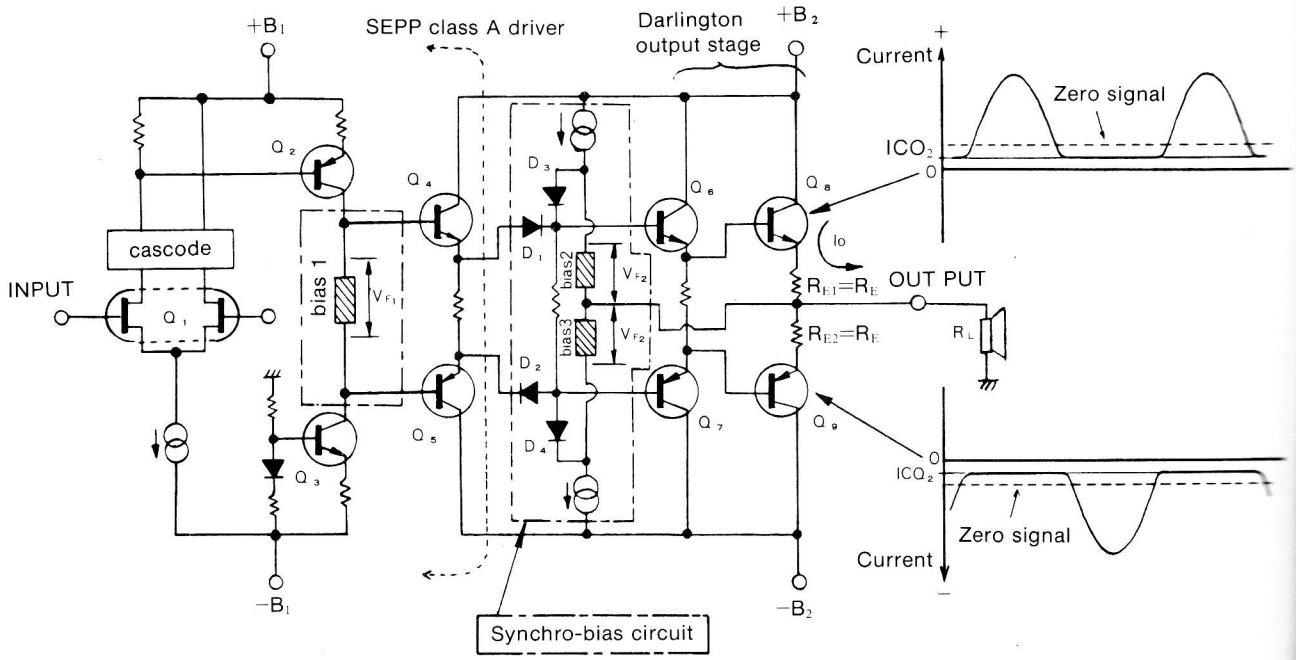
  This is the class A + system. This system, based on class A operation, has excellent features which cannot be achibved with conventional class A amps, with respect to efficiency and performance.

15-4. New Class A

The "new class A" having the low distortion of class A along with the efficiency of class B.



Technics "new class A"/synchro-bias circuit is set up so that the same fixed bias current is always flowing in both transistors during reproduction of both the positive and negative half cycles of the signal. Therefore, the output transistors never turn off, no matter what conditions of signal reproduction are present. Furthermore, the distortion-free quality of class A amps is achieved since there is no switching distortion and there is no nonlinearity in the load seen by the predriver voltage amp stage. Yet this "new class A" operation is accompanied by power conversion efficiency on a par with class B amplifiers.



[Fig. 15-25] "new class A" circuit

[Fig. 15-25] shows the entire circuit used in the new class A amplifier; the block enclosed by the dotted line is the synchro-bias circuit which is the key to the success of this revolutionary configuration.

The FET differential (Q_1) cascode first stage and voltage amp Q_2 with constant current load Q_3, along with SEPP-connected transistor Q_4 and Q_5 use bias 1 for class A operation as an emitter follower output stage driver circuit.

Bias 2 is for the positive half cycle output stage, and bias 3 is for the negative half cycle output stage, so that forward bias is always applied to the driver and output transistors so they are never turned off. Bias 2 and 3 are set at exactly the same voltage V_{F2} so that a fixed current will be supplied by the stabilized current supply circuitry.

During zero signal conditions the quiescent current, I_{CQ}, which flow in the Q_8 and Q_9 output transistors is the sum of I_{CQ_1} determined by bias 1, and I_{CQ_2} determined by bias 2 and 3.

Therefore, $I_{CQ} = I_{CQ1} + I_{CQ2}$

Where,

$$I_{CQ1} = \frac{V_{F1} - (V_{BE4} + V_{BE5} + V_{BE6} + V_{BE7} + V_{BE8} + V_{BE9} + V_{D1} + V_{D2})}{2R_E}$$

$$I_{CQ2} = \frac{2V_{F2} - (V_{BE6} + V_{BE7} + V_{BE8} + V_{BE9} + V_{D3} + V_{D4})}{2R_E}$$

. . . formula 2

When a signal is being reproduced, if, for example, the signal is swinging through the positive half-cycle, the current I_O will flow in the positive side of the output stage, and the voltage generated across the emitter resistance will be $R_{E1} \times I_O$.

Therefore, the negative output side's collector current determined by bias 1 will decrease but because bias 3 operates as a fixed voltage source, the quiescent current I_{CQ2} across the base emitter junctions of Q_7 and Q_9 will be maintained by forward bias so that the transistors will not be turned off.

The same thing happens during reproduction of the negative half cycles since bias 2 provides forward bias for positive output transistors Q_6 and Q_8 so that quiescent current I_{CQ2} is maintained.

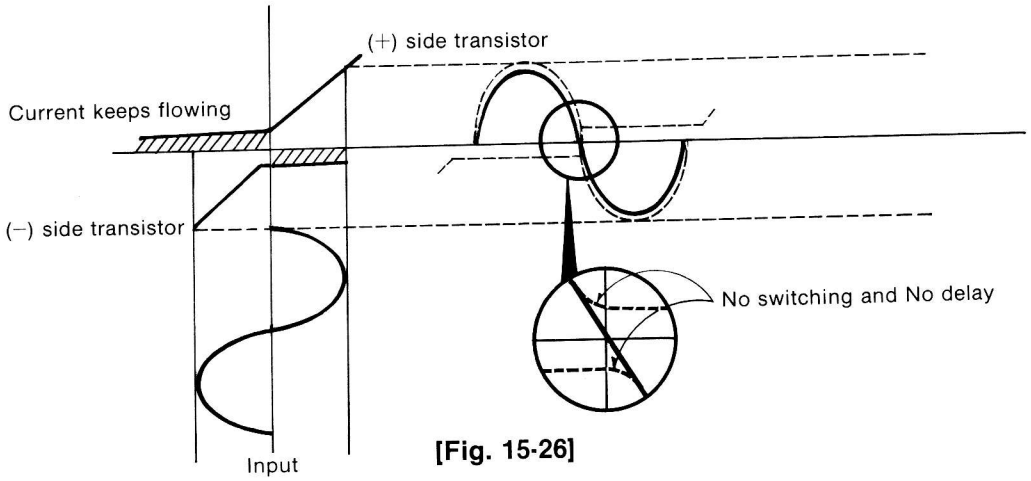
Because none of the transistors switch on and off there is no switching distortion generated during signal reproduction.

In addition, the load seen by Q_4 and Q_5 varies very little during positive and negative signal swings, even at the zero cross-point. At the same time, Q_4 and Q_5 operate in a class A emitter follower so that the voltage amp (Q_2) operates into a load having no nonlinearity. The result is that the circuit as a whole offers performance that is equivalent to class A amps yet completely eliminates the problems of class B amps.

In the synchro-bias circuit, the diodes D_1 and D_2 through which the signal passes, and the other diodes D_3 and D_4 through which the current for nonswitching output transistor operation during signal reproduction passes, are all high speed diodes which precisely follow the signal, even at high frequencies.

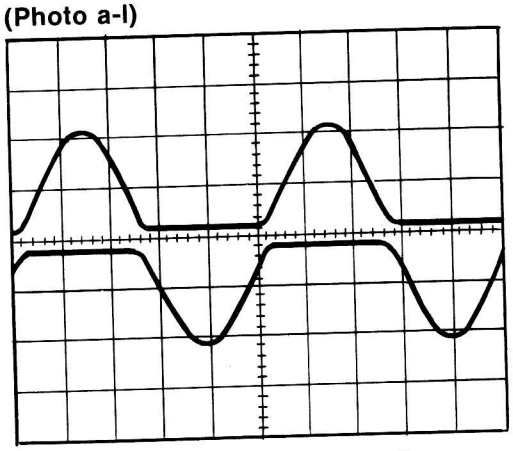
Bias 2 and Bias 3 operate in such a way that the positive and negative signal swings and zero cross-points are perfectly synchronized, and it is from this synchronization that we have given the circuit its name "synchro-bias".

Employing SLPT's (super linear power transistors), high speed diodes, and other advanced semiconductor technology, along with our concentrated power block configuration to prevent electromagnetic induction distortion, this "new class A" power amplifier as an entire component performs with the same outstanding quality that until now has been possible only with class A amps.



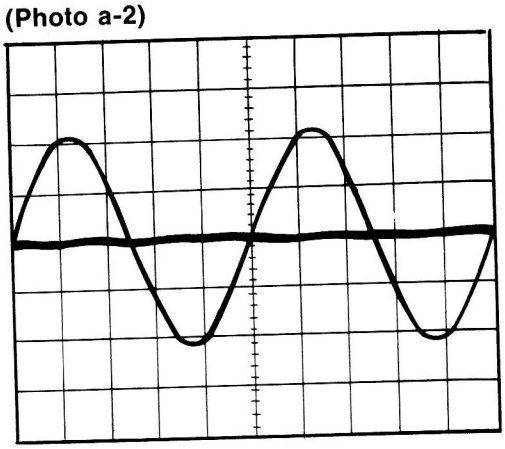
[Fig. 15-26]

(Photo a-l)



Output transistor current waveform

(Photo a-2)



Output signal waveform and distortion

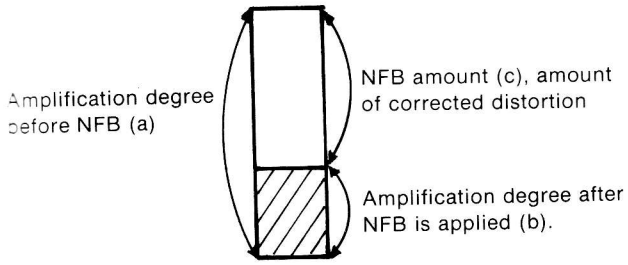
16. ADDITIONAL CIRCUITS

16-1. Feedback Circuit

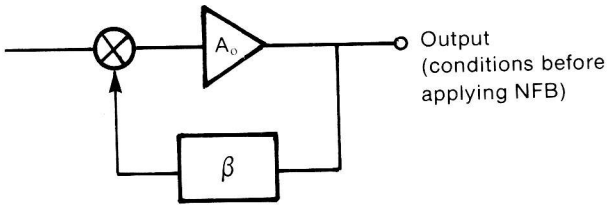
With feedback, part of the output signal of the amplifier is fed back to the input terminal and added with the original signal to improve the electrical characteristics of the amplifier.

(1) NFB (Negative feed back)

NFB is a control technique necessary to reduce the distortion of an amplifier. When a transistor amplifies a signal, the input waveform and output waveform do not always coincide. This is the cause of distortion. With negative feedback, a part of the amplified signal is fed back to the input side and the output waveform is compared with the input waveform. If distortion is generated, there is a change in the shape of the input waveform and output waveform, and an attempt is made to correct it so that: input waveform = output waveform.



[Fig. 16-1]



[Fig. 16-2]

A_{NF} (amplification degree after applying NFB)

$$= \frac{A_o}{1 + A_o \cdot \beta} = \frac{1}{\frac{1}{A_o} + \beta} \qquad \therefore A_o = \infty \quad A_{NF} = \frac{1}{\beta}$$

A_o : amplification degree
A_o : distortion
D_o : output impedance
β : NFB circuit

Z_{NF} (output impedance after applying NFB)

$$= \frac{Z_o}{1 + A_o \cdot \beta} = \frac{\frac{Z_o}{A_o}}{\frac{1}{A_o} + \beta} \qquad \therefore A_o = \infty \quad Z_{NF} = \frac{0}{\beta} = 0$$

D_{NF} (distortion after applying NFB)

$$= \frac{D_o}{1 + A_o \cdot \beta} = \frac{\frac{D_o}{A_o}}{\frac{1}{A_o} + \beta} \qquad \therefore A_o = \infty \quad D_{NF} = \frac{0}{\beta} = 0$$

Although Ao $= \infty$ is assumed in the above equations, this assumption is necessary for an ideal NFB amp. If Ao is infinitely large, an ideal NFB amp will be realized with distortion = 0, output impedance = 0 (damping factor).

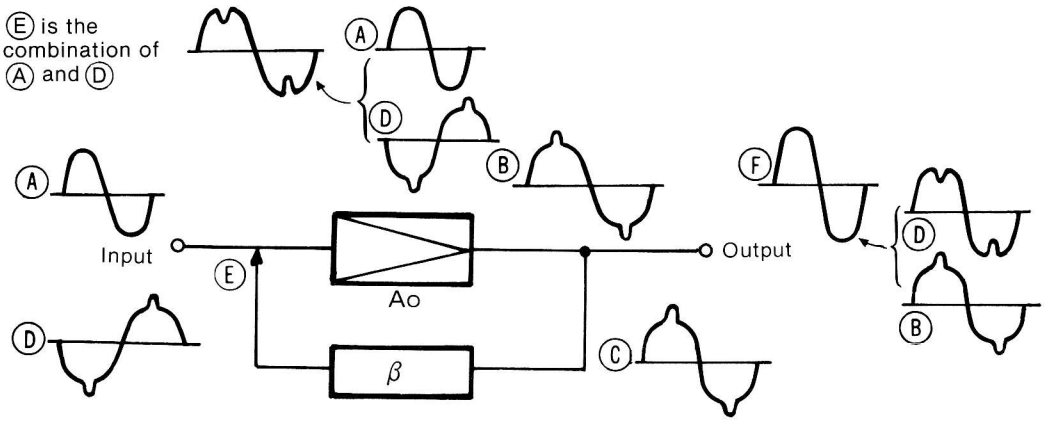
In reality Ao $= \infty$ is not obtainable. (Ao is usually $10^4 \sim 10^5$)

However even if Ao is a finite value, the distortion becomes

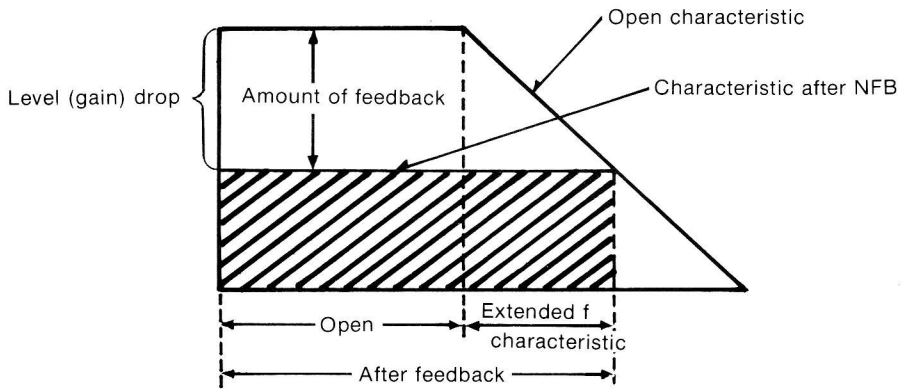
$$D_{NF} = \frac{D_0}{1 + A_o \beta}$$

and is greatly improved. The larger Ao is, the closer D_{NF} approaches 0.

Until now, output waveform Ⓑ was obtained by amplifying a distortion-free waveform Ⓐ with Ao.
Now, a part of Ⓑ is taken (waveform Ⓒ), is passed through feedback circuit β and has its polarity reversed (waveform Ⓓ).
Combining it with input waveform Ⓐ results in waveform Ⓔ
If this signal is amplified with Ao, which distorts it like waveform Ⓑ, a signal similar to waveform Ⓕ is output. The amplifier gain decreases by the amount of NFB since part of the output is sent back to the input.
Since the frequency characteristic extends by the amount of the decrease, the frequency range is greatly improved compared to the open characteristics.



[Fig. 16-3]



[Fig. 16-4] Comparison of the open characteristic and the characteristic after NFB.

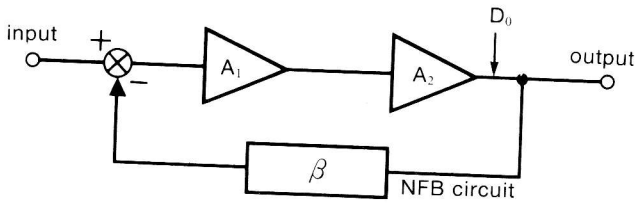
(2) PFB (positive feedback)

When a signal is fed back in-phase with the input signal, the gain increases.
A part of this increased output is sent to the input in the same proportion and is then added to the input signal. As a result, the signal increases even more.
In the electrical circuit, this feedback is repeated instantly many times and the output of the amp is increased to infinity.

(3) LEB (Linear Feedback)

a) Principle of LFB Amplification

It will be convenient to consider the ideal NFB amp as represented below, where A_1 and A_2 replace A_0.



A_1=1st stage gain
A_2=2nd stage gain
D_0=distortion without NFB
Z_0=output impedance without NFB

[Fig. 16-5]

If it is possible to make A_1 infinite, $A_1.A_2$ will also be infinite. When NFB is applied to such an amp, ideal characteristics can obtained, and distortion will drop to zero.

○ A_{NF} (GAIN WITH NFB)

$$= \frac{A_1 \cdot A_2}{1 + A_1 \cdot A_2 \cdot \beta} = \frac{1}{\frac{1}{A_1 \cdot A_2} + \beta} = \frac{1}{\frac{1}{\infty} + \beta} = \frac{1}{\beta}$$

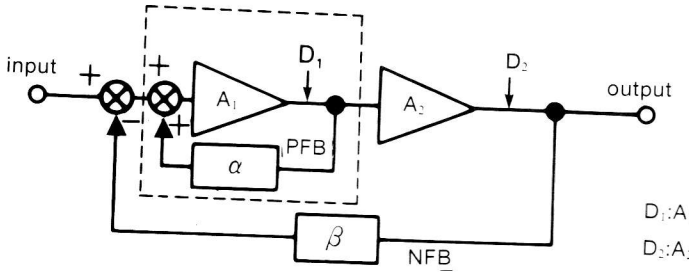
○ Z_{NF} (OUTPUT IMPEDANCE WITH NFB)

$$= \frac{Z_0}{1 + A_1 \cdot A_2 \cdot \beta} = \frac{Z_0}{1 + \infty \cdot \beta} = \frac{Z_0}{\infty} = 0$$

○ D_{NF} (DISTORTION WITH NFB)

$$= \frac{D_0}{1 + A_1 \cdot A_2 \cdot \beta} = \frac{D_0}{1 + \infty \cdot \beta} = \frac{D_0}{\infty} = 0$$

Let us examine positive feedback (PFB) as a possible means of obtaining infinite A_1.



D_1:A_1 amp distortion without PFB
D_2:A_2 amp distortion without PFB

[Fig. 16-6]

The 1st stage (dotted line will have a gain determined as

$$A_{1PF} = \frac{A_1}{1 - A_1 \cdot \alpha}$$